REMARKS

I. Introduction

In response of the Office Action dated October 4, 2005, Applicant has amended the specification so as to correct the inaccurate reference numerals assigned to the SRAM and DRAM. No new matter has been entered.

Further, it is noted that the Examiner has not provided an initialed copy of the Information Disclosure Statement deposited with the instant application filed on November 2, 2001. A copy of the IDS and stamped-post card showing receipt by the PTO is attached hereto for the Examiner's reference. It is respectfully requested that the Examiner provide the Applicant an initialed copy of the IDS indicating that each of the prior art references cited therein have been considered and made of record.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-2, 5 and 8-9 Under 35 U.S.C. § 103

Claims 1-2, 5 and 8-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of USP No. 6,691,206 to Rubinstein. Applicant respectfully requests reconsideration of this rejection for at least the following reasons.

Claims 1 and 8

A. The AAPA and Rubinstein Do Not Disclose A Lookup Table

Claim 1 recites in-part a router adapted to route data to one or more output devices, the router including a router table and implemented as a DRAM and SRAM ***lookup table***.

In the pending rejection, the Examiner admits that the AAPA does not disclose using both DRAM and SRAM in a lookup table, and relies on the DRAM array shown in Fig. 6 and col. 7, line 3 of Rubinstein to cure this deficiency.

However, it is respectfully submitted that Rubinstein still fails to arrive at the claimed invention, because the SRAM cells used as part of the DRAM array as disclosed in Rubinstein cannot ***functionally*** be considered equivalent to a ***lookup table***.

The Examiner is directed to **M.P.E.P. § 2111** *et seq.*, which mandates that claim limitations must be interpreted in light of the specification and afforded the plain meaning given by *those of ordinary skill in the art.*

In the instant case, the lookup table as disclosed in Applicant's specification may be used to determine where the incoming packets are to be routed (see, page 4, lines 27-28). In contrast, the SRAM cells and DRAM array of Rubenstein are expressly employed to provide a synchronization handshake with the memory centric controller (MCC) and storage for the data (see, col. 7, lines 43-49).

Further, Rubinstein structurally differentiates over the claimed lookup table by preventing random access to any location in the DRAM array (see, col. 7, lines 49-51). That is, while claim 1 recites that the router is adapted to conduct a search of the SRAM and DRAM lookup table (e.g., anywhere in the lookup table), Rubenstein expressly prohibits such access of the SRAM cells/DRAM array. Accordingly, the memory structure as disclosed in Rubenstein, at best, may be used as buffer-like arrays, and certainly cannot be used as a lookup table for routing data to a corresponding output (e.g., based on the destination addresses stored in the lookup table).

In this regard, it should be noted that Rubenstein discloses that the bits of data of a row are ***sequentially*** allocated (see, col. 7, line 12) into SRAM cells and a DRAM array. That is, Rubenstein further distinguishes over the claimed invention, because searching and looking up the SRAM cells or DRAM array would no longer be necessary, as data is allocated and arranged in a sequential fashion. This is also supported by the express principle of operation disclosed in Rubinstein; namely, "... the input data is directed through MUX multiplexer 90 into a demultiplexer 89 which in turn ***directs*** individual words of data into ***successive locations*** in a wide latch 88 until the latch is filled (see, col. 8, lines 2-5)."

For at least the foregoing reasons, it is respectfully submitted that the SRAM cells/DRAM array as disclosed in Rubinstein cannot reasonably be construed as a lookup table.

The Examiner is directed to **M.P.E.P § 2143.03** under the section entitled "All Claim Limitations Must Be Taught or Suggested," which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (emphasis added) (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, it is respectfully submitted that claim 1 is patentable over the AAPA in view of Rubinstein because the proposed combination fails the "all the claim limitations" standard required under 35 U.S.C. § 103.

CLAIM 8

With respect to claim 8, this claim is directed to a method comprising providing a router adapted to route data to one or more output devices, the router including a router table and the router table implemented as a DRAM and DRAM ***lookup table***. Accordingly, for analogous reasons discussed above with respect to claim 1, it is respectfully submitted that claim 8 is also allowable over the AAPA and Rubinstein, taken alone or in combination.

CLAIM 5

A. The AAPA and Rubinstein Do Not Disclose Determining Accessing The DRAM Only If Necessary

Claim 5 recites in-part using a routing identification information for accessing an SRAM portion of a routing table for routing information, and ***if necessary***, a DRAM portion of the routing table.

However, as discussed *supra*, while Rubinstein may arguably show a DRAM array containing SRAM cells, it is respectfully submitted that Rubinstein is completely silent as to determining if accessing the DRAM array 40 ***is necessary*** prior to utilizing the DRAM array.

Indeed, Rubinstein expressly discloses a selective use of SRAM cells such that while the first bits (leading edge bits) of a row are allocated to SRAM cells so that these bits may be transferred at SRAM access speed, the remaining bits of the row are allocated onto the wide latches 86/88 using the DRAM array. That is, Rubinstein expressly ***requires*** the use of DRAM array and SRAM cells, so that the notion of determining whether accessing the DRAM array 40 is ***necessary*** is evidently not disclosed. Therefore, the allegation that Rubinstein discloses accessing the DRAM array 40 only if necessary is clearly unfounded.

In contrast, claim 5 requires accessing the DRAM portion of the routing table only if it is necessary. That is, the DRAM portion of the routing table may not be accessed at all if it is found unnecessary.

Accordingly, for at least these reasons, Applicant respectfully submits that the AAPA and Rubinstein, taken alone or in combination, do not disclose or suggest accessing a DRAM portion after determining accessing the DRAM portion is necessary, as recited in claim 5.

B. *The AAPA and Rubinstein Do Not Disclose functional inter-relationship between Alleged Data Packet Of The AAPA and The Alleged Routing Information of Rubinstein*

Further, claim 5 recites in-part ***routing data packet using routing information*** accessed through a SRAM portion (and DRAM if necessary).

As a preliminary matter, the pending rejection has neither identified how the DRAM array and SRAM cells are accessed in the disclosure of Rubinstein nor addressed how a data packet disclosed in the AAPA is routed using any routing information retrieved from the DRAM array and SRAM cells of Rubinstein. In this regard, it appears that the pending rejection improperly relies on two different processes (one directed to routing data packets, and another directed to interfacing SRAM buffer to DRAM array for bandwidth matching) as allegedly

disclosing the claimed method, when in fact, the relied on processes of the AAPA and that of Rubinstein are ***independent*** from one another so as to have ***no*** functional/conditional relationship therebetween. Accordingly, the allegation that a SRAM/DRAM memory and a data packet are well-known ***separately*** is irrelevant to the determination of patentability for the ***combination*** thereof.

In other words, the proposed combination at best discloses a ***functionally separated*** data packet and a SRAM/DRAM array. None of the cited prior art discloses a functional ***inter-relationship*** between routing identification information (e.g., by reading a header of a data packet), accessing a SRAM (and a DRAM if necessary), and routing a data packet using a routing information (e.g., retrieved through the SRAM or DRAM), as is evidenced by an absence of the inter-relationship between the data packet of the AAPA and the DRAM array of Rubinstein (i.e., routing data packet of the AAPA using routing information retrieved/accessed through the DRAM array of Rubinstein). Absent a showing of this inter-relationship, it is respectfully submitted that the proposed combination is based solely on improper hindsight reasoning, whereby the Examiner selected bits and pieces of the prior art and used only Applicant's specification as a guide to reconstruct the claimed invention.

Accordingly, for at least these foregoing reasons, even if the applied references are combined as suggested by the Examiner, and Applicant does not agree that the requisite fact-based motivation has been established, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).* Applicant, therefore, submits that the rejection of claims 1, 5 and 8 under 35 U.S.C. §103(a) for obviousness predicated upon the AAPA in view of Rubinstein is not factually accurate, and withdrawal of the rejection is respectfully requested.

III. The Rejection Of Claim 12 Under 35 U.S.C. § 103

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of Rubinstein, and further in view of USP No. 5,875,206 to Jones. Applicant respectfully traverses this rejection for at least the following reasons.

A. The AAPA, Rubinstein and Jones Do Not Disclose A Routing Controller

Furthermore, claim 12 recites that a routing controller uses routing identification information to access a ***routing table*** for routing information.

Again, even assuming *arguendo* that a routing controller is disclosed in the cited prior art, Applicant respectfully submits that the Examiner has not provided factual evidence to support how such routing controller, if disclosed, would access the DRAM array in the manner alleged.

In fact, it is respectfully submitted that the logic in making the proposed combination is flawed. Specifically, in order to support the allegation that the AAPA can be modified to include the DRAM array as disclosed in Rubinstein, Rubinstein should at least demonstrate that the DRAM array can be accessed by a routing controller for retrieving routing information (e.g., routing information associated with a packet). However, as Rubinstein is completely silent with regard to any routing information stored in the DRAM array 40 or a routing controller, it is respectfully submitted that the proposed combination is based solely on improper hindsight reasoning, utilizing Applicant's specification inadvertently as a guide to pick and choose the selected elements from various references so as to reach the claimed invention.

That is, even assuming Rubinstein is relevant, Rubinstein discloses only that a DRAM array may contain SRAM cells, but does not disclose or suggest accessing such table for routing information using the routing identification information retrieved from data packets of the AAPA. Absent a showing of the ***inter-relationship*** between data packet and routing identification information thereof in the AAPA, and the DRAM array of Rubinstein, it is not entirely understood how Rubinstein cures the deficiencies of the AAPA, given that the claimed routing table, routing controller, routing identification information and routing information as recited in claim 12 are ***inter-related***. At best, the rejection shows only that the ***individual***

elements of the claimed invention are known without providing a ***prima facie*** showing of obviousness that the combination of elements is known or suggested.

For all of the foregoing reasons, even if the applied references are combined, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). Applicant, therefore, submits that the rejection of claim 12 under 35 U.S.C. §103(a) for obviousness predicated upon the AAPA in view of Rubinstein and Jones is not factually accurate, and withdrawal of the rejection is respectfully requested.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is neither anticipated nor rendered obvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987).* Accordingly, as independent claims 1, 5, 8 and 12 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

V. Conclusion

By responding in the foregoing remarks only to particular positions taken by the Examiner, the Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

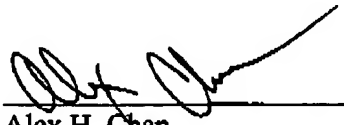
For all of the reasons set forth above, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: 12/23/05



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